[10191/1867]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:		: Examiner: Robert Fennema
	Rainer Sommer	:
For:	METHOD FOR CONTROLLING THE PROGRAM RUN IN A MICROCONTROLLER	:
Filed:	July 2, 2001	: Art Unit: 2183
Serial No.:	**09/897,870**	:

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

SIR:

In the above-identified patent application ("the present application"), Appellants mailed a Notice Of Appeal on July 20, 2007 (it was filed on July 23, 2007) from the Final Office Action issued by the U.S. Patent and Trademark Office on February 20, 2007, so that the two-month appeal brief due date is September 23, 2007, which has been extended by four (4) months to January 23, 2008 by the accompanying Transmittal and Petition to Extend.

In the Final Office Action, claims 1 to 32 were finally rejected. A Response After A Final Office Action was mailed on May 22, 2007, and an Advisory Action was mailed on June 8, 2007.

It is understood for purposes of the appeal that any Amendments to date have already been entered by the Examiner, and that the Response After Final does not require entry since it included no amendments.

As to the length of the "concise explanation" of the subject matter defined in each of the claims involved in the appeal (see 41.37), the "concise explanation" language is like the "concise explanation" requirement of former Rule 37 C.F.R. § 1.192. Accordingly, the

length of the concise explanation provided is acceptable, since it would have been acceptable under 37 C.F.R. § 1.192 and since it specifically defines the subject matter of the independent claims involved and in the appeal. In the filing of many appeal briefs under the old rule for the present Assignee, the length of the "concise explanation" has always been ultimately accepted by the Patent Office.

It is therefore respectfully submitted that this Appeal Brief complies with 37 C.F.R. § 41.37. Although no longer required by the rules, this Brief is submitted in triplicate as a courtesy to the Appeals Board.

It is respectfully submitted that the final rejections of claims 1 to 32 should be reversed for the reasons set forth below.

1. REAL PARTY IN INTEREST

The real party in interest in the present appeal is Robert Bosch GmbH ("Robert Bosch") of Stuttgart in the Federal Republic of Germany. Robert Bosch is the assignee of the entire right, title and interest in the present application.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences or other appeals related to the present application, which "will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal".

3. STATUS OF CLAIMS

A. Claims 1 to 4, 6 to 8, 10 to 14 and 16 to 32 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 4,489,414 to Titherley in view of the Plug and Play ISA Specification, by Intel and Microsoft, and further in view of "Transforming the PC: Plug and Play" by Halfhill.

B. Claims 5, 9 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over the "Titherley" reference in view of the "Plug and Play" reference and further in view of U.S. Patent No. 6,182,203 to Simar et al.

Appellants therefore appeal from the final rejections of pending and considered claims 1 to 32. A copy of all of the pending and considered and appealed claims 1 to 32 is attached hereto in the Claims Appendix.

4. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on February 20, 2007, Appellants filed a Response After A Final Office Action (with no amendments), which was mailed on May 22, 2007.

It is understood for purposes of the appeal that any Amendments to date have already been entered by the Examiner, and that the Response After Final does not require entry since it included no amendments.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The concise explanation of the summary of the claimed subject matter is as follows, as described in the context of the present application.

As in claim 1 and 32, the specification and Figures disclose and describe the following:

The "Background Information" section explains that there are microcontrollers that include at least one microprocessor, an analog/digital (A/D) converter, a digital/analog (D/A) converter, a databus, internal control elements (e.g. a read only memory), and/or additional components. The different versions of one microcontroller within one controller family are referred to as controller steps, which can have different scopes of functionalities (so called features) and/or different faulty features (which are bypassed by way of so called workarounds, in which case an attempt is made to simulate the faulty features using other features). Because of the different features and workarounds, the programs according to the related art are adapted to the particular controller step, but the result is a plurality of different programs that all have to be maintained during software updates. (See specification, page 1, line 11 to page 2, line 2).

The presently claimed subject matter provides the benefit of flexibility, so that it is possible to control the run of a program executable on at least one microprocessor of a microcontroller to the greatest extent possible, so that the program can be flexibly adapted to the different controller steps of a microcontroller. It is particularly advantageous that the presently claimed subject matter proposes that information regarding the hardware of the microcontroller be read in from at least one information register of a microcontroller, and that, as a function of the information read in, at least one switch be actuated via which the run of the program is controlled. (See specification, page 3, line 17 to 25).

As to claims 1 (6, 10 and 32), they are to a method or device for controlling a run of a program executable on at least one microprocessor of a microcontroller, In Figure 1, a microcontroller 1 having a microprocessor 2, an internal storage element 3, an analog/digital (A/D) converter 4, and a databus 5. Information regarding the hardware of the microcontroller is stored in an information register 6 of microcontroller 1. (See specification, page 7, lines 15 to 19). The presently claimed subject matter provides the control program is controlled as a function of the information regarding the hardware of microcontroller 1 stored in information register 6 (see Figure 3). After the method is started in block 30, information regarding the hardware of microcontroller 1 is first read in from information register 6 in block 31. In block 32, switches are set as a function of the information read in. Subsequently, the control program is executed with the set switches in block 33, and is ended in block 34. (See specification, page 8, lines 11 to 18).

As to claim 1 (6, 10 and 32), they also include the feature of reading in information regarding hardware of the microcontroller from at least one information register of the microcontroller. In this regard, the run of the test program is controlled as a function of the information regarding the hardware of microcontroller 1 stored in information register 6. After the method is started in block 30, information regarding the hardware of microcontroller 1 is read in from information register 6 in block 31 (see Figure 3). (See specification, page 9, lines 25 to 29).

As to claim 1(6, 10 and 32), they also include the feature of actuating at least one switch via which the program run is controlled as a function of the information read in. In this regard, the method according to the presently claimed subject matter of claim 1 provides for switches, via which the run of the test program can be influenced, are set as a function of the information read in (see Figure 3, functional block 32). (See specification, page 9, lines 30 to 31).

As to claim 1 (and 6 and 10), it further includes the feature in which program execution only depends on information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences. In this regard, the specification discloses that the method

provides for the test program to be executed with the set switches in block 33, and is ended in block 34 (see Figure 3). (See specification, page 9, lines 32 to 33).

As to claim 32, it analogously includes the feature in which the program is executable using at least two different microcontroller steps, and that in the at least one information register of the microcontroller, the information directly relates to hardware of a special microcontroller step and that, depending on this information, execution of the program is switchable so that only program parts are executed which are necessary for the special microcontroller step, so that the execution of the program is directly related to the special microcontroller step. In this regard, the specification discloses that the method provides for the execution of the program using, different microcontroller steps wherein the test program can be particularly simply and reliably configured in correspondence with the particular microcontroller step, and can be accordingly controlled. (See specification, page 5, lines 10 to 13).

As to claim 6, the specification and Figures disclose and describe the following:

As to claim 6, it is to a control element for one of a control unit of an internal combustion engine, the control element including a microcontroller, and a testing device for testing at least one of the microcontroller, the control unit including the microcontroller, and a program executable on at least one microprocessor of the a microcontroller. The specification discloses that the control element is provided for a control unit (*including in a motor vehicle, as in claims 5, 9 and 15*) may be in a motor vehicle or for a testing device for testing a microcontroller, a control unit, and/or a program executable on at least one microprocessor of the microcontroller. (See specification, page 5, line 31 to page 6, line 1).

As to claim 6, it further includes a storage medium storing a program sequence that can be executed on a computing element. The specification discloses that the a program that can be executed on a computing element, in particular on a microprocessor, and is suitable for carrying out the method is stored in the control element. (See specification, page 6, lines 1 to 4 and lines 7 to 8).

As to claim 6, it further provides for the computing element to: read in information regarding hardware of the microcontroller from at least one information register of the microcontroller, and actuate at least one switch via which a program run is controlled as a function of the information read in; in which program execution only depends on information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences. Thus, the method of claim 1 is implemented by a program stored on the control element, so that this control element provided with the program represents the presently claimed subject matter in the same manner as the method for whose implementation the program is suited. (See specification, page 6, lines 4 to 6).

As to claim 10 the specification and Figures disclose and describe the following:

As to claim 10, it is to a *microcontroller, comprising at least one microprocessor including a program that is executable on the at least one microprocessor and at least one information register.* In Figure 1, a microcontroller has a microprocessor 2, an internal storage element 3, an analog/digital (A/D) converter 4, and a databus 5, and information regarding the hardware of the microcontroller is stored in an information register 6 of microcontroller 1. (See specification, page 7, lines 15 to 19).

As to claim 10, it further provides for an arrangement for reading in information regarding hardware of the microcontroller from the at least one information register; and at least one switch actuatable as a function of the information read in and for controlling a run of the program executable on the at least one microprocessor; in which program execution only depends on the information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences. To achieve the object of the presently claimed subject matter, the microcontroller includes an arrangement reading in information regarding the hardware of one microcontroller from at least one information register of the microcontroller, as well as at least one switch actuatable as a function of the information read in, for controlling the run of the program executable on the at least one microprocessor of the microcontroller. (See specification, page 6, lines 10 to 14).

As to dependent claims 5, 9 and 15, they further require that their base claim features be used in the context of a motor vehicle. The specification discloses, for example, that the control element is provided for a control unit (*including in a motor vehicle, as in claims 5, 9 and 15*) may be in a motor vehicle or for a testing device for testing a microcontroller, a control unit, and/or a program executable on at least one microprocessor of the microcontroller. (See specification, page 5, line 31 to page 6, line 1).

In particular, claim 5 ultimately depends from claim 1, and provides that the technical operations and processes relate to a motor vehicle; claim 9 depends from claim 6 and provides that the internal combustion engine is of a motor vehicle; and claim 15 ultimately depends from claim 1, and provides that the technical operations and processes relate to a motor vehicle. (See claims 5, 9 and 15)

In summary, the presently claimed subject matter is to a method for controlling a run of a program executable on at least one microprocessor of a microcontroller, including: reading in information regarding hardware of the microcontroller from at least one information register of the microcontroller; and actuating at least one switch via which the program run is controlled as a function of the information read in; wherein program execution only depends on information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences. (See claim 1).

In summary, the presently claimed subject matter is to a control element for one of a control unit of an internal combustion engine, the control element including a microcontroller, and a testing device for testing at least one of the microcontroller, the control unit including the microcontroller, and a program executable on at least one microprocessor of the a microcontroller, the control element comprising: a storage medium storing a program sequence that can be executed on a computing element, the program sequence causing the computing element to: read in information regarding hardware of the microcontroller from at least one information register of the microcontroller, and actuate at least one switch via which a program run is controlled as a function of the information read

in; in which program execution only depends on information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences. (See claim 6).

In summary, the presently claimed subject matter is to a microcontroller, including: at least one microprocessor including a program that is executable on the at least one microprocessor; at least one information register; an arrangement for reading in information regarding hardware of the microcontroller from the at least one information register; and at least one switch actuatable as a function of the information read in and for controlling a run of the program executable on the at least one microprocessor; in which program execution only depends on the information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences. (See claim 10).

In summary, the presently claimed subject matter is to a method for controlling a run of a program executable on at least one microprocessor of a microcontroller, including: reading in information regarding hardware of the microcontroller from at least one information register; and actuating at least one switch via which the program run is controlled as a function of the information read in; in which the program is executable using at least two different microcontroller steps, and that in the at least one information register of the microcontroller, the information directly relates to hardware of a special microcontroller step and that, depending on this information, execution of the program is switchable so that only program parts are executed which are necessary for the special microcontroller step, so that the execution of the program is directly related to the special microcontroller step. (See claim 32).

Finally, the appealed claims include no means-plus-function language and no step-plus-function claims, so that 37 C.F.R. 41.37(v) is satisfied as to its specific requirements for such claims, since none are present here. Also, the present application does not contain any step-plus-function claims because the method claims in the present application are not "step plus function" claims because they do not recite "a step for", as required by the Federal Circuit and as stated in Section 2181 of the MPEP.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1 to 4, 6 to 8, 10 to 14 and 16 to 32 under 35 U.S.C. § 103(a) are unpatentable over U.S. Patent No. 4,489,414 to Titherley in view of the Plug and Play ISA Specification, by Intel and Microsoft, and further in view of "Transforming the PC: Plug and Play" by Halfhill.

B. Whether claims 5, 9 and 15 under 35 U.S.C. § 103(a) are unpatentable over the "Titherley" reference in view of the "Plug and Play" reference and further in view of U.S. Patent No. 6,182,203 to Simar et al.

7. ARGUMENT

A. The rejections under 35 U.S.C. § 103(a) as to Claims 1 to 4, 6 to 8, 10 to 14 and 16 to 32

Claims 1 to 4, 6 to 8, 10 to 14 and 16 to 32 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 4,489,414 to Titherley in view of the Plug and Play ISA Specification, by Intel and Microsoft, and further in view of "Transforming the PC: Plug and Play" by Halfhill. The responses to date are incorporated by reference, as appropriate.

In rejecting a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a *prima facie* case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Still further, the prior art must disclose or suggest each claim feature and it must also provide a motivation or suggestion for combining the features in the manner contemplated by the claim. (See Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990), cert. denied, 111 S. Ct. 296 (1990); In re Bond, 910 F.2d 831, 834 (Fed. Cir. 1990)). Thus, the "problem confronted by the inventor must be considered in determining whether it would have been obvious to combine the references in order to solve the problem", Diversitech Corp. v. Century Steps, Inc., 850 F.2d 675, 679 (Fed. Cir. 1998).

It is respectfully submitted that the Office Actions to date have not established a *prima facie* case of obviousness. Specifically, there is no valid motivation to combine the "Titherley" reference with either the "Plug and Play" reference or the "Halfhill" reference.

The nature of the subject matter of the "Titherly," "Plug and Play" and "Halfhill" references is such that it would not be obvious to one of ordinary skill in the art to modify the "Titherley" reference using either the "Plug and Play" reference or the "Halfhill" reference. Generally speaking, the "Titherley" reference is directed to testing computer peripherals with portable test equipment. At any one time, the portable test equipment is only attached to one peripheral under test, or at most a plurality of serially attached devices, such as the daisy-chained devices of col. 5, lines 1-5.

In contrast, the "Plug and Play" reference is directed to arbitrating conflicting demands for system resources by a plurality of cards attached to an ISA bus. The plurality of cards are all simultaneously attached to the ISA bus, creating a situation in which the plurality of ISA cards are effectively attached in parallel. Thus, the aim and technological bent of the "Plug and Play" reference is to arbitrate simultaneous requests from a plurality of parallel devices. Accordingly, it would not be obvious to one of ordinary skill in the art to apply such a technology arbitrating simultaneous and parallel requests, as in the "Plug and Play" reference, to the single or serial device situation of the "Titherley" reference because one of ordinary skill in the art would not consider applying a technology created for parallel devices to a situation involving a single or serial devices. That is, there are no conflicting requests for system resources in the "Titherley" reference, and therefore one of ordinary skill in the art would not be motivated to apply a technology for resolving such parallel resource request conflicts to a situation that did not involve parallel resource request conflicts.

Still further, it is respectfully submitted that the motivation to combine the references provided in the Final Office Action of February 20, 2007 and the Advisory Action of June 8, 2007 is not valid in the context of modifying the "Titherley" reference with either the "Plug and Play" or the "Halfhill" references, and thus does not provide proper motivation to combine these references. Regarding the motivation to combine, the Final Office Action states on page 5 that "*it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying plug and play functionality to Titherley would be able to reduce the complexity of the system, which is a burden* ***to the user****, and thus automate the system.*"

Further regarding the motivation to combine, the Advisory Action states (in the continuation of 11) that "*it will make PCs easier to set up and configure*" and that "*it will ease the task of installing new hardware and software.* " However, one skilled in the art would not be motivated to modify the "Titherly" reference to apply plug-and-play functionality because the "Titherly" reference in fact teaches away from this combination. The "Titherly" reference, for example, stresses the importance of the of reducing the complexity of the system by altering the programming of the testing devise by changing plug-in program modules and thereby *avoiding the use of a general purpose computer* due to the cost and unwieldiness of such a computer as an engineer's diagnostic tool. (See col. 1, lines 44 to 50).

Furthermore, the "Titherly" reference refers to a "hand carried device" which would form part of a maintenance engineer's equipment. It is submitted that applying the plug-and-play functionality would greatly increase the complexity of the system of the "Titherley" reference in this context. For example, the portable test equipment of the "Titherley" reference would need to be modified and enhanced to communicate with plug-and-play devices in a manner that would accomplish the "Plug and Play" functionality (for example, steps 1-7 as in FIG. 2 on page 5 of the "Plug and Play" reference) which is significantly more complex than the manner in which the "Titherley" reference already communicates with the peripheral under test. This would be in stark contrast to the stated goal of the "Titherley" reference to have a system which "is as simple and as cheap as possible in the sense that many features of existing microprocessor systems which are irrelevant to peripheral testing

and exercising are omitted." (See col. 2, lines 36 to 41). In fact the "Titherley" reference goes further suggesting that "It will be apparent that such portable microprocessor system is effectively inoperable as a computer system in the absence of the plug-in firmware module." Thus, the portable test equipment of the "Titherley" reference, if modified by the "Plug and Play" reference, would greatly increase in complexity and not function for its intended use as a portable diagnostic tool.

Therefore, contrary to the unsupported assertions of the Office Actions to date, one of ordinary skill in the art would be dissuaded from modifying the "Titherley" reference with the "Plug and Play" reference to make PCs easier to set up and configure or to ease the task of installing new hardware and software -- due to the "Titherley" reference's teaching away from this increased complexity, which would be burdensome in the design, manufacture and use of the portable test equipment for its intended purpose.

Also, it is respectfully submitted that there would also be no motivation to modify the "Titherley" reference with either the "Plug and Play" or the "Halfhill" references because such a modification would not actually even provide any benefit to a user of the portable test equipment of the "Titherley" reference. The Office is respectfully reminded that, as stated in the MPEP at section 2143.01.III, "*[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination*" (some emphasis added). The device of the "Titherley" reference is not a PC and the peripherals that the device of the "Titherley" reference were intended to test are not plug-and-play enabled peripherals.

In fact, the device of the "Titherley" reference is capable (with the proper plug-in module) of testing peripherals which do not even include an Industry Standard Architecture (ISA) card as required for plug-and-play to function. Thus, even if the portable test equipment of the "Titherley" reference were modified to work with plug-and-play peripherals, it would not provide any increased functionality to the portable test equipment because the device of the "Titherley" reference is not a PC and does not test plug-and-play peripherals. Accordingly, one of ordinary skill in the art would not be motivated to combine the "Titherley" reference with the "Plug and Play" and "Halfhill" references because it would not be desirable to do so because there would be no benefit.

As stated in the MPEP at section 2141.02.VI, "*[a] prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention*" (some emphasis added). Furthermore, it would at least be overly burdensome to modify all of the devices that the "Titherley" reference is intended to test to be plug-and-play enabled. For evidence of the incredible difficulty of such a task, the Office is directed to the "Halfhill" reference, which discusses this at length. The "Halfhill" references states of page 1, for example, "*And although Plug and Play does a remarkable job of making PCs friendlier while maintaining compatibility with existing hardware, it also requires that you eventually replace almost all that hardware.*" In the Advisory Action (at the continuation of 11), the Office asserts that this reference has been taken out of context and that the many advantages of plug-and-play far outweigh the stipulation that you must eventually replace old, obsolete hardware, however Applicants disagree. Within the context of the "Titherley" reference, this requirement to replace all hardware would be burdensome, as conceded by the Office in the Advisory Action (at the continuation of 11), and would not provide any benefit because the device of the "Titherley" reference is not a PC and does not test plug-and-play peripherals. Consequently, one of ordinary skill in the art would be dissuaded from modifying the "Titherley" reference.

Since the references are not properly combinable, they cannot and do not disclose a method for controlling a run of a program executable on at least one microprocessor of a microcontroller, including: reading in information regarding hardware of the microcontroller from at least one information register of the microcontroller; and actuating at least one switch via which the program run is controlled as a function of the information read in, including the feature in which *program execution only depends on information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences*, as provided for in the context of claim 1 (and in claims 6 and 10).

This is also true for essentially the same reasons as to claim 10, which analogously (but more specifically) provides that the "*program is executable using at least two different microcontroller steps, and that in the at least one information register of the microcontroller, the information directly relates to hardware of a special microcontroller step and that,*

depending on this information, execution of the program is switchable so that only program parts are executed which are necessary for the special microcontroller step, so that the execution of the program is directly related to the special microcontroller step".

Accordingly, claims 1, 6, 10 and 32 are allowable, as are their dependent claims.

Still further, it is respectfully submitted that the cases of In re Fine, supra, and In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992), make plain that the Office's generalized assertions that it would have been obvious to modify or combine the references do not properly support a § 103 rejection. It is respectfully submitted that those cases make plain that the Office's assertions reflect a subjective "obvious to try" standard, and therefore does not reflect the proper evidence to support an obviousness rejection based on the references relied upon. In particular, the Court in the case of In re Fine stated that:

> The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. This it has not done. . . .
>
> **Instead, the Examiner relies on hindsight in reaching his obviousness determination. . . . One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.**

In re Fine, 5 U.S.P.Q.2d at 1598 to 1600 (citations omitted; italics in original; emphasis added). Likewise, the Court in the case of In re Jones stated that:

> Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. . . .
>
> **Conspicuously missing from this record is any evidence, other than the PTO's speculation (if it be called evidence) that one of ordinary skill . . . would have been motivated to make the modifications . . . necessary to arrive at the claimed [invention].**

In re Jones, 21 U.S.P.Q.2d at 1943, 1944 (citations omitted; italics in original).

That is exactly the case here since it is believed and respectfully submitted that the Office Actions to date offer no evidence whatsoever, but only conclusory hindsight, reconstruction and speculation, which these cases have indicated does not constitute evidence that will support a proper obviousness finding. Unsupported assertions are not evidence as to why a person having ordinary skill in the art would be motivated to modify or combine references to provide the claimed subject matter of the claims to address the problems met thereby, as explained above.

Indeed, the Federal Circuit in the case of In re Kotzab has made plain that even if a claim concerns a "technologically simple concept" — which is not the case here — there still must be some finding as to the "specific understanding or principle within the knowledge of a skilled artisan" that would motivate a person having no knowledge of the claimed subject matter to "make the combination in the manner claimed," stating that:

> In this case, the Examiner and the Board fell into the hindsight trap. The idea of a single sensor controlling multiple valves, as opposed to multiple sensors controlling multiple valves, is a technologically simple concept. With this simple concept in mind, the Patent and Trademark Office found prior art statements that in the abstract appeared to suggest the claimed limitation. But, there was no finding as to the specific understanding or principle within the knowledge of a skilled artisan that would have motivated one with no knowledge of Kotzab's invention to make the combination in the manner claimed. In light of our holding of the absence of a motivation to combine the teachings in Evans, we conclude that the Board did not make out a proper prima facie case of obviousness in rejecting [the] claims . . . under 35 U.S.C. Section 103(a) over Evans.

In re Kotzab, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000) (emphasis added). Here again, there have been no such findings to establish that the features discussed above of the rejected claims are met by the reference relied upon. As referred to above, any review of the references, whether taken alone or combined, makes plain that the references do not describe the features discussed above of the rejected claims.

Therefore, there is no valid motivation to combine the "Titherley," "Plug and Play" and "Halfhill" references in view of Simar, U.S. Patent No. 6,182,203, so that independent claims 1, 6, 10 and 32, as well as their respective dependent claims 2 to 4, 7 to 8, 11 to 14 and 16 to 31, are allowable.

B. The Rejections Under 35 U.S.C. § 103(a) as to Dependent Claims 5, 9 and 15

Claims 5, 9, and 15 respectively depend from independent claims 1, 6 and 10, but require that the features be used in the context of a motor vehicle, and are therefore allowable over the "Titherley" reference in view of the "Plug and Play" reference for essentially the reasons explained above as to their base claims.

Moreover, the third-level "Simar" reference does not cure – and is not asserted to cure -- the critical deficiencies of the primary and secondary references as explained above.

Therefore, claims 5, 9, and 15 are allowable over the "Titherley" reference in view of the "Plug and Play" reference and also in view of the "Simar" reference.

As further regards all of the obviousness rejections of the claims, *the presently claimed subject matter provides the benefit of flexibility, so that it is possible to control the run of a program executable on at least one microprocessor of a microcontroller to the greatest extent possible, so that the program can be flexibly adapted to the different controller steps of a microcontroller. It is particularly advantageous that the presently claimed subject matter proposes that information regarding the hardware of the microcontroller be read in from at least one information register of a microcontroller, and that, as a function of the information read in, at least one switch be actuated via which the run of the program is controlled*. (See specification, page 3, line 17 to 25). Accordingly, the claimed subject matter is not obvious since its benefits are evidence of non-obvious as to the references as applied.

As still further regards all of the obviousness rejections of the claims, it is respectfully submitted that a proper *prima facie* case has not been made in the present case for

obviousness, since the Office Actions to date never made any findings, such as, for example, regarding in any way whatsoever what a person having ordinary skill in the art would have been at the time the claimed subject matter of the present application was made. (See *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998) (the "factual predicates underlying" a *prima facie* "obviousness determination include the scope and content of the prior art, the differences between the prior art and the claimed invention, and the level of ordinary skill in the art")). It is respectfully submitted that the proper test for showing obviousness is what the "combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art", and that the Patent Office must provide particular findings in this regard — the evidence for which does not include "broad conclusory statements standing alone". (See *In re Kotzab*, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000) (citing *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1618 (Fed. Cir. 1999) (obviousness rejections reversed where no findings were made "concerning the identification of the relevant art", the "level of ordinary skill in the art" or "the nature of the problem to be solved"))). It is respectfully submitted that there has been no such showings by the Office Actions to date or by the Advisory Action.

In fact, the present lack of any of the required factual findings forces both Appellants and any Appeals Board to resort to unwarranted speculation to ascertain exactly what facts underly the present obviousness rejections. The law mandates that the allocation of the proof burdens requires that the Patent Office provide the factual basis for rejecting a patent application under 35 U.S.C. § 103. (See *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A. 1967))). In short, the Examiner bears the initial burden of presenting a proper prima facie unpatentability case — which has not been met in the present case. (See *In re Oetiker*, 977 F.2d 1443, 1445, 24, U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992)).

Accordingly, claims 1 to 32 are allowable.

CONCLUSION

In view of the above, it is respectfully requested that the rejections of the finally rejected claims 1 to 32 be reversed, and that these claims be allowed as presented.

Respectfully submitted,

Dated: 1/23/2008

By: _____

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CLAIMS APPENDIX

1. (Previously Presented) A method for controlling a run of a program executable on at least one microprocessor of a microcontroller, comprising the steps of:

reading in information regarding hardware of the microcontroller from at least one information register of the microcontroller; and

actuating at least one switch via which the program run is controlled as a function of the information read in;

wherein program execution only depends on information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences.

2. (Original) The method according to claim 1, wherein:

the information read in corresponds to at least one of the at least one microprocessor of the microcontroller and at least one additional component of the microcontroller.

3. (Previously Presented) The method according to claim 1, further comprising the step of:

controlling a run of a test program that is executable on the at least one microprocessor of the microcontroller of a testing device and is for testing at least one of an additional microcontroller, a control unit including the additional microcontroller, and a control program executable on at least one microprocessor of the additional microcontroller, the controlling being performed as a function of information regarding hardware of the additional microcontroller.

4. (Original) The method according to claim 1, further comprising the step of:

controlling a run of a control program that is executable on the at least one microprocessor of the microcontroller of a control unit and is for controlling/regulating technical operations and processes, the controlling being performed as a function of the information regarding the hardware of the microcontroller.

5. (Original) The method according to claim 4, wherein:

the technical operations and processes relate to a motor vehicle.

6. (Previously Presented) A control element for one of a control unit of an internal combustion engine, the control element including a microcontroller, and a testing device for testing at least one of the microcontroller, the control unit including the microcontroller, and a program executable on at least one microprocessor of the a microcontroller, the control element comprising:

a storage medium storing a program sequence that can be executed on a computing element, the program sequence causing the computing element to:

read in information regarding hardware of the microcontroller from at least one information register of the microcontroller, and

actuate at least one switch via which a program run is controlled as a function of the information read in;

wherein program execution only depends on information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences.

7. (Previously Presented) The control element according to claim 6, wherein:

the computing element includes at least one microprocessor.

8. (Original) The control element according to claim 6, wherein:

the storage medium includes one of a read only memory and a flash memory.

9. (Original) The control element according to claim 6, wherein:

the internal combustion engine is of a motor vehicle.

10. (Previously Presented) A microcontroller, comprising:

at least one microprocessor including a program that is executable on the at least one microprocessor;

at least one information register;

an arrangement for reading in information regarding hardware of the microcontroller from the at least one information register; and

at least one switch actuatable as a function of the information read in and for controlling a run of the program executable on the at least one microprocessor;

wherein program execution only depends on the information in the at least one information register of the microcontroller, which is special for each microcontroller step, without other external or operator related influences.

11. (Original) The microcontroller according to claim 10, wherein:

the information read in corresponds to at least one of the at least one microprocessor of the microcontroller and at least one additional component of the microcontroller.

12. (Original) The microcontroller according to claim 11, wherein:

the information regarding the at least one additional component of the microcontroller includes information about at least one of an internal storage element, an analog/digital (A/D) converter, a digital/analog (D/A) converter, and at least one databus.

13. (Original)The microcontroller according to claim 10, wherein:

the microcontroller is part of a testing device for testing at least one of an additional microcontroller, a control unit, and the program executable on the at least one microprocessor.

14. (Original) The microcontroller according to claim 10, wherein:

the microcontroller is part of a control unit for controlling/regulating technical operations and processes.

15. (Original) The microcontroller according to claim 14, wherein:

the technical operations and processes relate to a motor vehicle.

16. (Previously Presented) The method according to claim 2, wherein:

the information regarding the at least one additional component of the microcontroller includes information about at least one of an internal storage element, an analog/digital (A/D) converter, a digital/analog (D/A) converter, and at least one databus.

17. (Previously Presented) The control element according to claim 6, wherein:

the information read in corresponds to at least one of the at least one microprocessor of the microcontroller and at least one additional component of the microcontroller.

18. (Previously Presented) The control element according to claim 17, wherein:

the information regarding the at least one additional component of the microcontroller includes information about at least one of an internal storage element, an analog/digital (A/D) converter, a digital/analog (D/A) converter, and at least one databus.

19. (Previously Presented) The method according to claim 1, wherein:

the program run is controlled by one of activating and deactivating at least one of command sequences for specific features of the microcontroller and workarounds.

20. (Previously Presented) The method according to claim 1, wherein:

the information read in corresponds to at least one of a manufacture, model, type and size of components of the microcontroller.

21. (Previously Presented) The control element according to claim 6, wherein:

the information read in corresponds to at least one of a manufacture, model, type and size of components of the microcontroller.

22. (Previously Presented) The microcontroller according to claim 10, wherein:

the information read in corresponds to at least one of a manufacture, model, type and size of components of the microcontroller.

23. (Previously Presented) The method according to claim 1, wherein the information is read in from a read-only information register.

24. (Previously Presented) The control element according to claim 6, wherein the information is read in from a read-only information register.

25. (Previously Presented) The microcontroller according to claim 10, wherein the information is read in from a read-only information register.

26. (Previously Presented) The method according to claim 1, wherein the program run occurs without external intervention for operating or displaying as to a program time sequence.

27. (Previously Presented) The control element according to claim 6, wherein the program run occurs without external intervention for operating or displaying as to a program time sequence.

28. (Previously Presented) The microcontroller according to claim 10, wherein the run of the program occurs without external intervention for operating or displaying as to a program time sequence.

29. (Previously Presented) The method according to claim 1, wherein there is only one control program for different hardware configurations.

30. (Previously Presented) The control element according to claim 6, wherein there is only one control program for different hardware configurations.

31. (Previously Presented) The microcontroller according to claim 10, wherein there is only one control program for different hardware configurations.

32. (Previously Presented) A method for controlling a run of a program executable on at least one microprocessor of a microcontroller, comprising:

reading in information regarding hardware of the microcontroller from at least one information register of the microcontroller; and

actuating at least one switch via which the program run is controlled as a function of the information read in;

wherein the program is executable using at least two different microcontroller steps, and that in the at least one information register of the microcontroller, the information

directly relates to hardware of a special microcontroller step and that, depending on this information, execution of the program is switchable so that only program parts are executed which are necessary for the special microcontroller step, so that the execution of the program is directly related to the special microcontroller step.

EVIDENCE APPENDIX

Appellants have not submitted any evidence pursuant to 37 CFR Sections 1.130, 1.131 or 1.132, and do not rely upon evidence entered by the Examiner.

RELATED PROCEEDINGS INDEX

There are no interferences or other appeals related to the present application.